MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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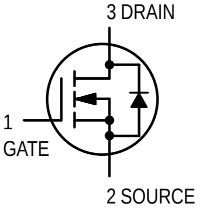
by 2N7002LT1/D

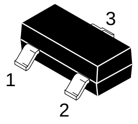
TMOS FET Transistor

N–Channel Enhancement

2N7002LT1

Motorola Preferred Device





CASE 318 – 08, STYLE 21
SOT– 23 (TO – 236AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Drain Current — Continuous T_C = 25°C(1) T_C = 100°C(1) — Pulsed(2)	I_D I_D I_{DM}	±115 ±75 ±800	mAdc
Gate–Source Voltage — Continuous — Non–repetitive ($t_p \le 50$ µs)	 V_{GS} V_{GSM}	 ±20 ±40	 Vdc Vpk

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board,(3) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate,(4) T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	–55 to +150	°C

DEVICE MARKING

2N7002LT1 = 702

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 10 µAdc)	$V_{(BR)DSS}$	60	—	—	Vdc
Zero Gate Voltage Drain Current T_J = 25°C (V_{GS} = 0, V_{DS} = 60 Vdc) T_J = 125°C	I_{DSS}	— —	— —	1.0 500	µAdc
Gate–Body Leakage Current, Forward (V_{GS} = 20 Vdc)	I_{GSSF}	—	—	100	nAdc
Gate–Body Leakage Current, Reverse (V_{GS} = –20 Vdc)	I_{GSSR}	—	—	–100	nAdc

1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.
3. FR–5 = 1.0 x 0.75 x 0.062 in.
4. Alumina = 0.4 x 0.3 x 0.025 in 99.5% alumina.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS(2)					
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = 250 μAdc)	$V_{GS(th)}$	1.0	—	2.5	Vdc
On–State Drain Current ($V_{DS} \geq 2.0\ V_{DS(on)}$, V_{GS} = 10 Vdc)	$I_{D(on)}$	500	—	—	mA
Static Drain–Source On–State Voltage	$V_{DS(on)}$				Vdc
(V_{GS} = 10 Vdc, I_D = 500 mAdc)		—	—	3.75	
(V_{GS} = 5.0 Vdc, I_D = 50 mAdc)		—	—	0.375	
Static Drain–Source On–State Resistance	$r_{DS(on)}$				Ohms
(V_{GS} = 10 V, I_D = 500 mAdc) T_C = 25°C		—	—	7.5	
T_C = 125°C		—	—	13.5	
(V_{GS} = 5.0 Vdc, I_D = 50 mAdc) T_C = 25°C		—	—	7.5	
T_C = 125°C		—	—	13.5	
Forward Transconductance ($V_{DS} \geq 2.0\ V_{DS(on)}$, I_D = 200 mAdc)	g_{FS}	80	—	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	50	pF
Output Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	—	25	pF
Reverse Transfer Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	—	5.0	pF
SWITCHING CHARACTERISTICS(2)					
Turn–On Delay Time (V_{DD} = 25 Vdc, $I_D \cong$ 500 mAdc, R_G = 25 Ω, R_L = 50 Ω)	$t_{d(on)}$	—	—	30	ns
Turn–Off Delay Time	$t_{d(off)}$	—	—	40	ns
BODY–DRAIN DIODE RATINGS					
Diode Forward On–Voltage (I_S = 11.5 mAdc, V_{GS} = 0 V)	V_{SD}	—	—	–1.5	Vdc
Source Current Continuous (Body Diode)	I_S	—	—	–115	mAdc
Source Current Pulsed	I_{SM}	—	—	–800	mAdc

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

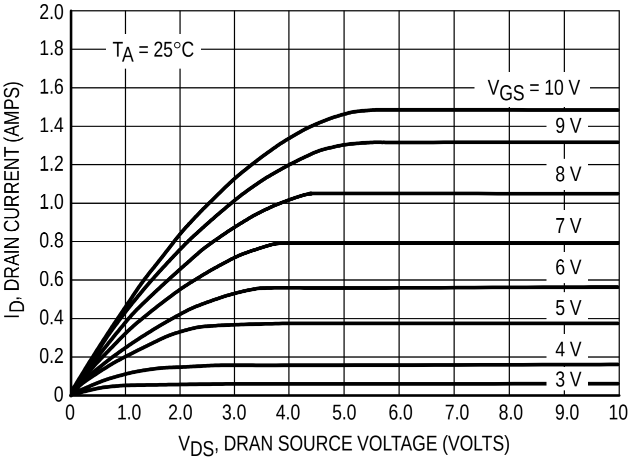


Figure 1. Ohmic Region

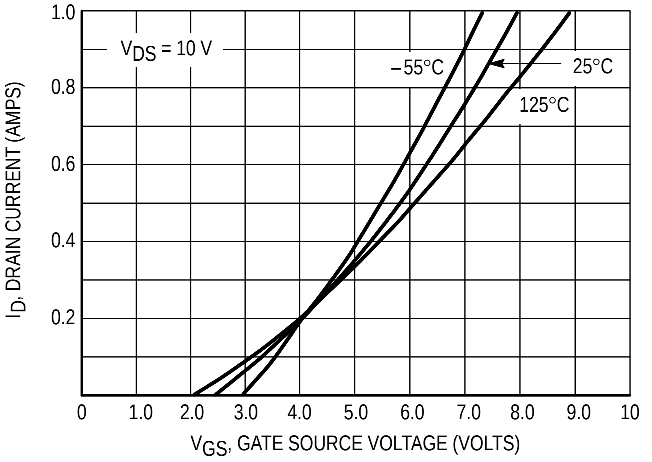


Figure 2. Transfer Characteristics

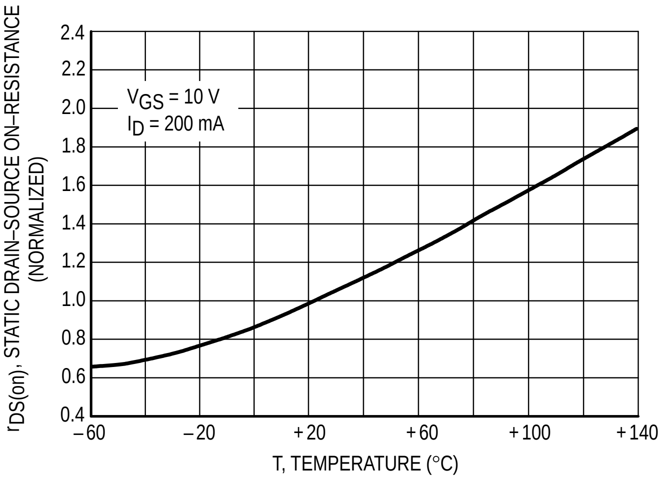


Figure 3. Temperature versus Static Drain–Source On–Resistance

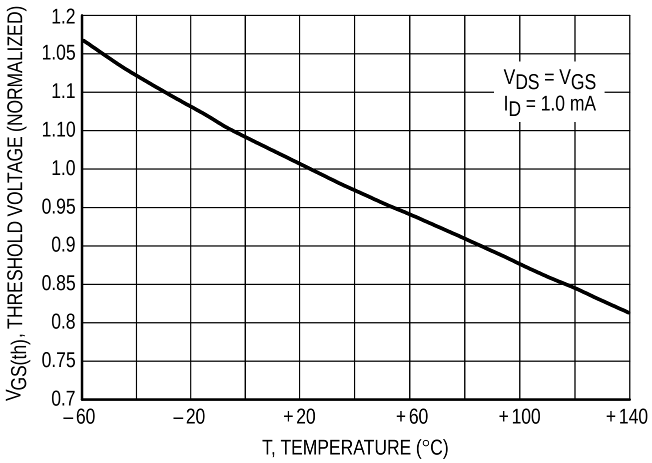
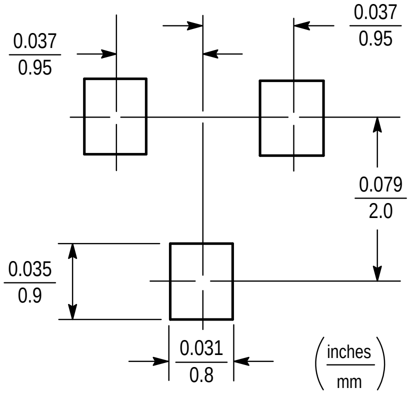


Figure 4. Temperature versus Gate Threshold Voltage

INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–23

SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

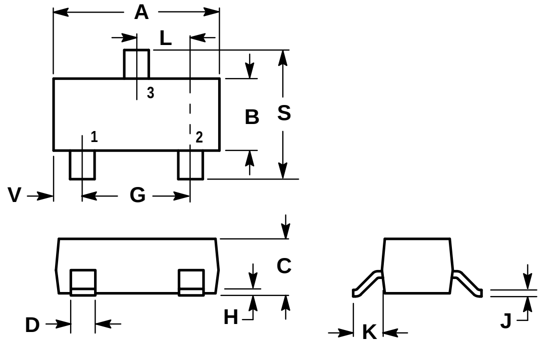
SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIUMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

CASE 318–08
ISSUE AF
SOT–23 (TO–236AB)

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