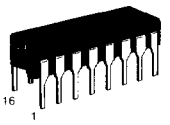
MOTOROLA

MC14029B

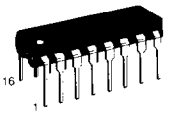
BINARY/DECADE UP/DOWN COUNTER

The MC14029B Binary/Decade up/down counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide toggle flip-flop capability. The counter can be used in either Binary or BCD operation. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

- Diode Proection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design – Count Occurs on Positive Going Edge of Clock
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin for Pin Replacment for CD4029B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648

D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

T_A = −55° to 125°C for all packages.

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MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

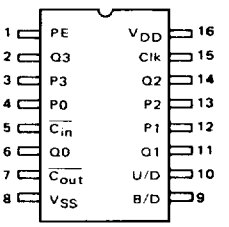
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C

TRUTH TABLE

$\overline{\text{Carry In}}$	Up/Down	Preset Enable	Action
1	X	0	No Count
0	1	0	Count Up
0	0	0	Count Down
X	X	1	Preset

X = Don't Care

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0	−3.0	—	−2.4	−4.2	—	−1.7	—	mAdc
		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
		10	−1.6	—	−1.3	−2.25	—	−0.9	—	
		15	−4.2	—	−3.4	−8.8	—	−2.4	—	
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.58 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.20 μA/kHz) f + I_{DD}							
		15	I_T = (1.70 μA/kHz) f + I_{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH},					ns
Clk to Q	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	—	200	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	—	90	180	
Clk to $\overline{C_{out}}$	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns	t_{PHL}	5.0	—	250	500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	—	85	190	
$\overline{C_{in}}$ to $\overline{C_{out}}$	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 95 ns	t_{PHL}	5.0	—	175	360	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 47 ns		10	—	50	120	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	—	50	100	
PE to Q	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns	t_{PHL}	5.0	—	235	470	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	—	80	160	
PE to $\overline{C_{out}}$	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns	t_{PHL}	5.0	—	320	640	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	—	145	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	—	105	210	
Clock Pulse Width	$t_{W(cl)}$	5.0	180	90	—	ns
		10	80	40	—	
		15	60	30	—	
Clock Pulse Frequency	f_{cl}	5.0	—	4.0	2.0	MHz
		10	—	8.0	4.0	
		15	—	10	5.0	
Preset Removal Time	t_{rem}	5.0	160	80	—	ns
The Preset Signal must be low prior to a positive-going transition of the clock.		10	80	40	—	
		15	60	30	—	
Clock Rise and Fall Time	$t_{r(cl)}$	5.0	—	—	15	μs
	$t_{f(cl)}$	10	—	—	5	
		15	—	—	4	
$\overline{Carry}$ In Setup Time	t_{su}	5.0	150	75	—	ns
		10	60	30	—	
		15	40	20	—	
Up/Down Setup Time		5.0	340	170	—	ns
		10	140	70	—	
		15	100	50	—	
Binary/Decade Setup Time		5.0	320	160	—	ns
		10	140	70	—	
		15	100	50	—	
Preset Enable Pulse Width	t_W	5.0	130	65	—	ns
		10	70	35	—	
		15	50	25	—	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

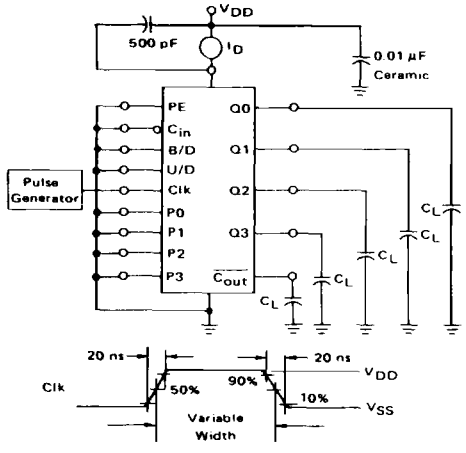
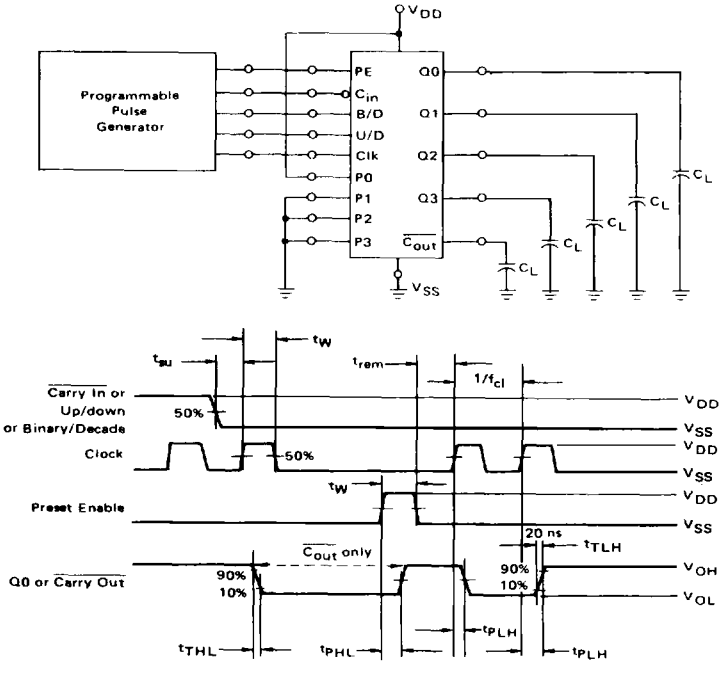


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



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TIMING DIAGRAM

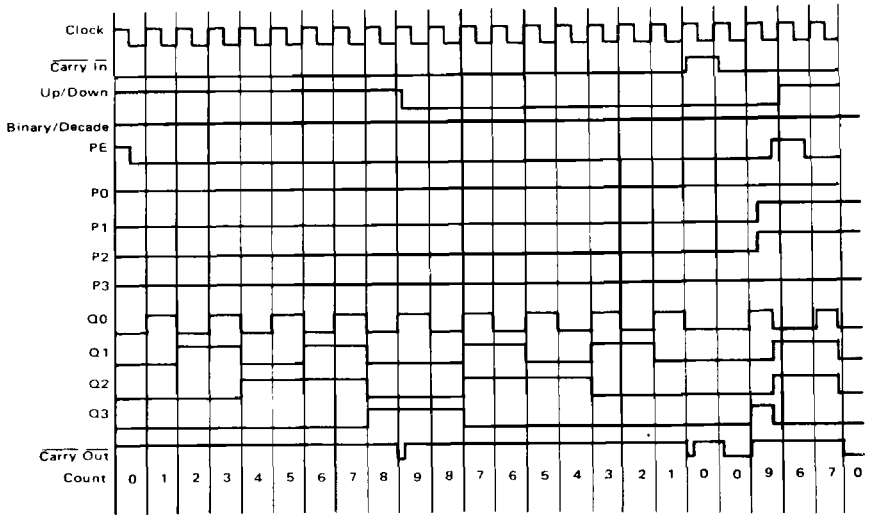
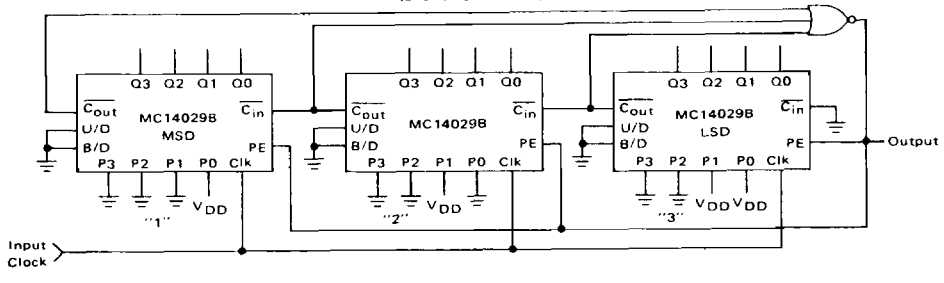
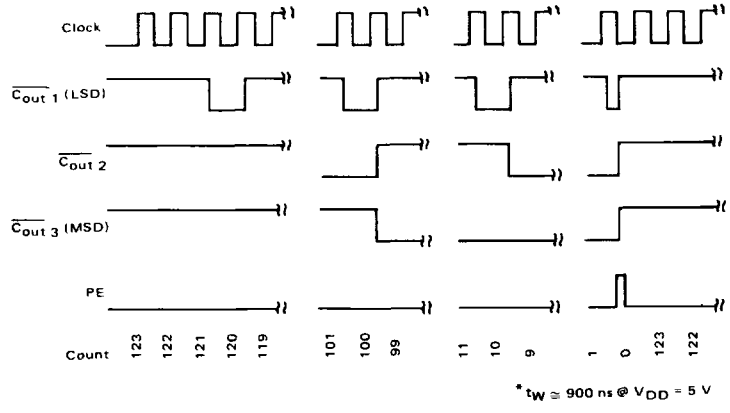


FIGURE 3 – DIVIDE BY N BCD DOWN COUNTER and TIMING DIAGRAM
(Shown for N = 123)





*$t_W \cong 900$ ns @ $V_{DD} = 5$ V

LOGIC DIAGRAM