Signetics

FAST 74F861, 74F862, 74F863, 74F864 Bus Transceivers

'F861/'F862 10-Bit Bus Transceivers, NINV/INV (3-State)
'F863/'F864 9-Bit Bus Transceivers, NINV/INV (3-State)
Product Specification

FAST Products

FEATURES

- **Provide high performance bus interface buffering for wide data/address paths or busses carrying parity**
- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **I_{IL} is 20μA vs 1000μA for AM29861 series**
- **Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors**
- **Positive and negative over-shoots are clamped to ground**
- **3-state outputs glitch free during power-up and power-down**
- **Slim Dip 300 mil package**
- **Broadside pinout compatible with AMD AM 29861-29864 series**
- **Outputs sink 64mA**

DESCRIPTION

The 74F861 series Bus Transceivers provide high performance bus interface buffering for wide data/address paths of busses carrying parity. The 'F863/'F864 9-bit Bus Transceivers have NOR-ed transmit and receive output enables for maximum control flexibility.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F861, 74F862	6.0ns	150mA
74F863, 74F864	6.0ns	115mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F861N, N74862N, 74F863N, N74F864N
24-Pin Plastic SOL[1]	N74F861D, N74F862D, 74F863D, N74F864D

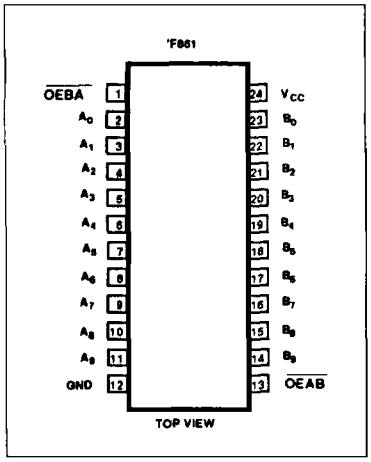
NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal considerations for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

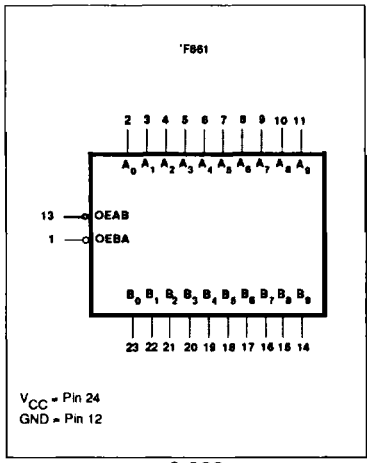
PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F861 'F862	A_0 - A_9	Data transmit inputs	3.5/0.117	70μA/70μA
	B_0 - B_9	Data receive inputs	3.5/0.117	70μA/70μA
	$\overline{OEBA}$	Transmit output enable input	1.0/0.033	20μA/20μA
	$\overline{OEAB}$	Receive output enable input	1.0/0.033	20μA/20μA
	A_0 - A_9	Data transmit outputs	1200/106.7	24mA/64mA
	B_0 - B_9	Data receive outputs	1200/106.7	24mA/64mA
'F863 'F864	A_0 - A_9	Data transmit inputs	3.5/0.117	70μA/70μA
	B_0 - B_9	Data receive inputs	3.5/0.117	70μA/70μA
	$\overline{OEBA}_n$	Transmit output enable inputs	1.0/0.033	20μA/20μA
	$\overline{OEAB}_n$	Receive output enable inputs	1.0/0.033	20μA/20μA
	A_0 - A_8	Data transmit outputs	1200/106.7	24mA/64mA
	B_0 - B_8	Data receive outputs	1200/106.7	24mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

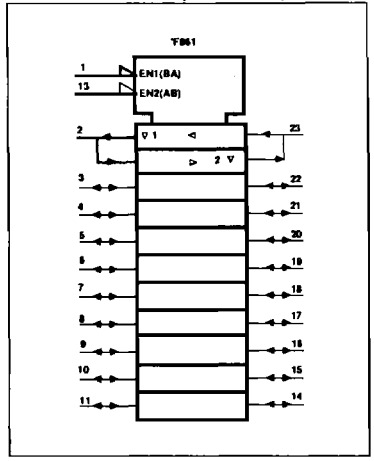
PIN CONFIGURATION



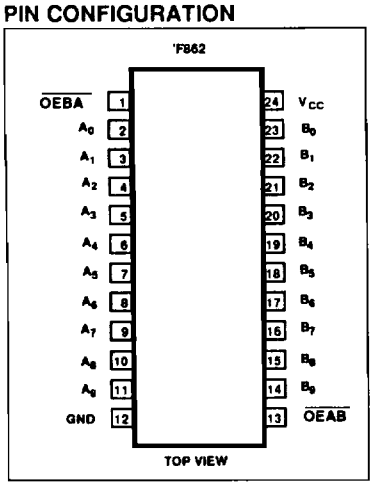
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



PIN CONFIGURATION



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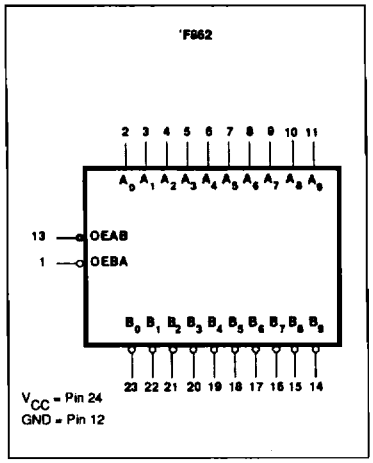

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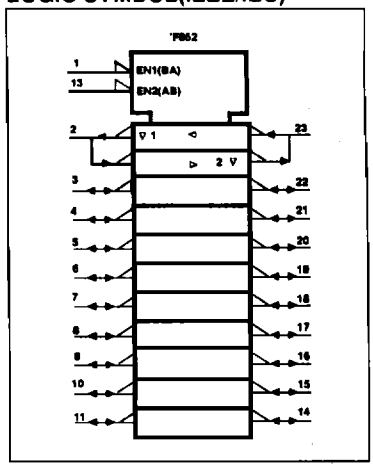

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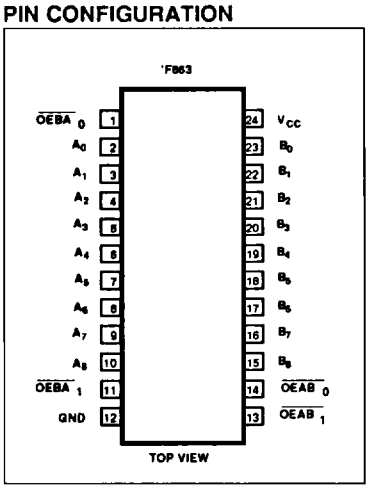

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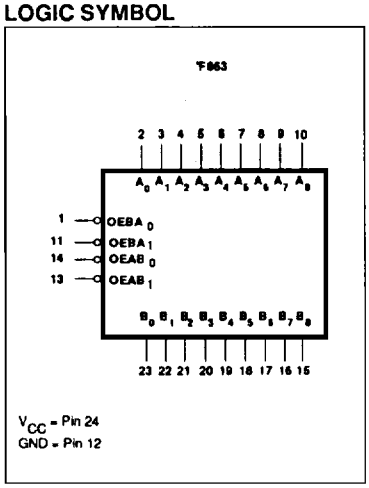

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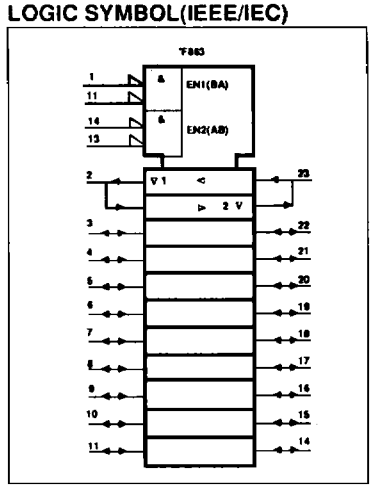

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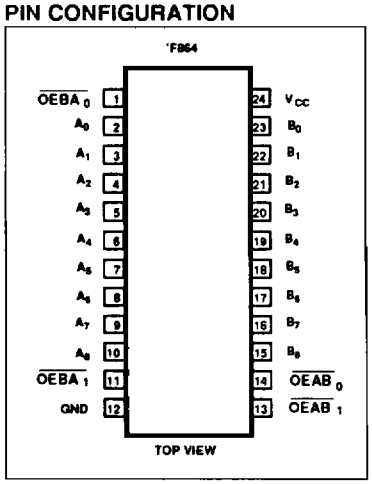

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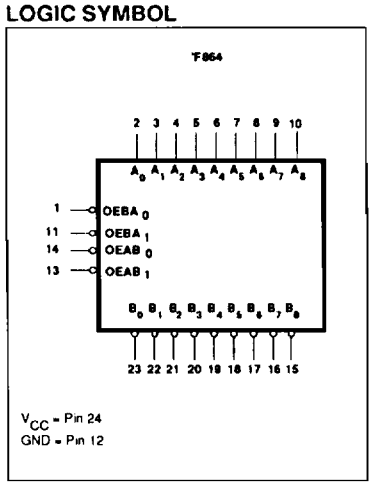

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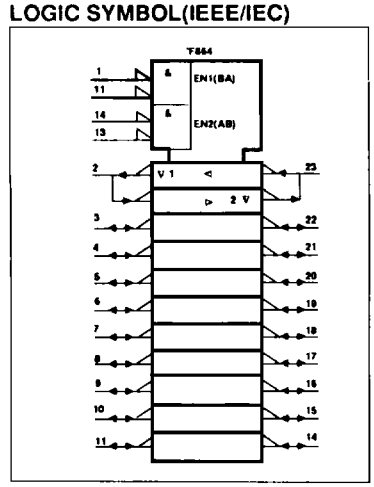
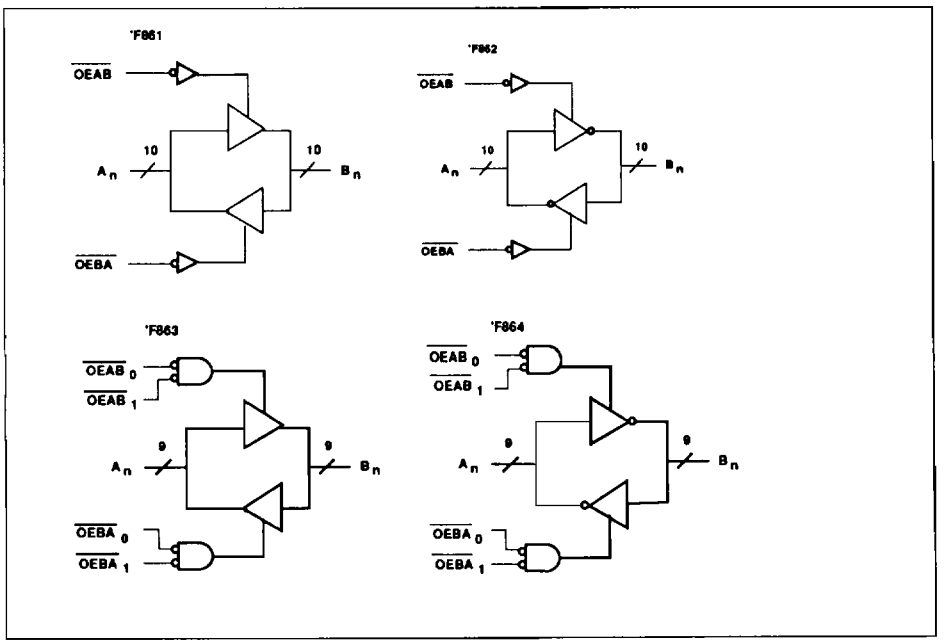


FUNCTION TABLE for 'F861 and 'F862

INPUTS		OPERATING MODES	
$\overline{OEAB}$	$\overline{OEBA}$	'F861	'F862
L	H	A data to B bus	A data to B bus
H	L	B bus to A data	B bus to A data
H	H	Z	Z

H = High voltage level
L = Low voltage level
Z = High impedance "off" state

LOGIC DIAGRAM



FUNCTION TABLE for 'F863 and 'F864

INPUTS				OPERATING MODES	
$\overline{OEAB}_0$	$\overline{OEAB}_1$	$\overline{OEBA}_0$	$\overline{OEBA}_1$	'F863	'F864
L	L	H	X	A data to B bus	A data to B bus
L	L	X	H		
H	X	L	L	B bus to A data	B bus to A data
X	H	L	L		
H	H	H	H	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-15mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.4	3.3		V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-24mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEAB}$, $\overline{OEBA}$ $\overline{OEAB}_n$, $\overline{OEBA}_n$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_n, B_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
$I_{IH}+I_{OZH}$	High-level input current	A_n, B_n	V_{CC} = MAX, V_O= 2.7V					70	µA
$I_{IL}+I_{OZL}$	Low-level input current	A_n, B_n	V_{CC} = MAX, V_O= 0.5V					-70	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F861 'F863	I_{CCH}	V_{CC} = MAX			145	195	mA
			I_{CCL}				140	195	mA
			I_{CCZ}				165	220	mA
		'F862 'F864	I_{CCH}	V_{CC} = MAX			90	130	mA
			I_{CCL}				120	170	mA
			I_{CCZ}				130	160	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

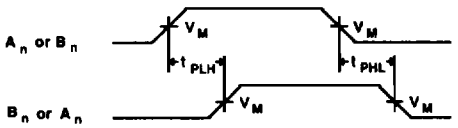
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F861, 74F863					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	4.0 3.0	6.0 5.0	9.0 8.0	3.5 2.5	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	4.0 2.5	6.0 5.0	9.0 8.0	3.5 2.5	10.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	6.0 4.5	8.0 7.0	11.5 10.5	5.0 4.5	13.0 12.0	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	6.0 5.5	8.0 7.5	11.0 11.0	5.0 4.5	13.0 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	3.5 2.5	5.5 5.0	9.0 8.5	3.0 2.0	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	3.5 2.5	5.5 4.5	8.5 8.5	3.0 2.0	9.5 9.5	ns

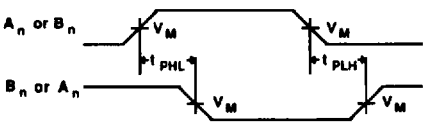
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F862, 74F864					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	4.0 1.5	6.0 3.5	9.0 6.5	3.0 1.5	10.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	4.0 1.5	6.0 3.5	9.0 6.5	3.0 1.5	10.5 7.0	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	6.5 7.0	8.5 9.5	12.0 13.5	5.5 6.0	13.5 15.5	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	6.5 7.5	8.0 9.5	11.5 13.5	5.5 6.5	13.5 15.5	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns

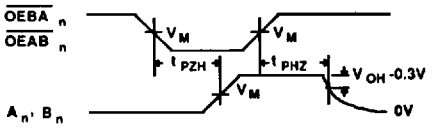
AC WAVEFORMS



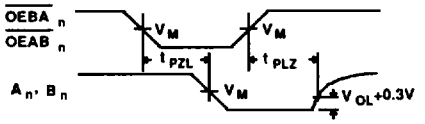
Waveform 1. Propagation Delay For Non-Inverting Output



Waveform 2. Propagation Delay For Inverting Output



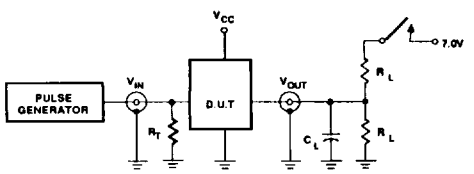
Waveform 3 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

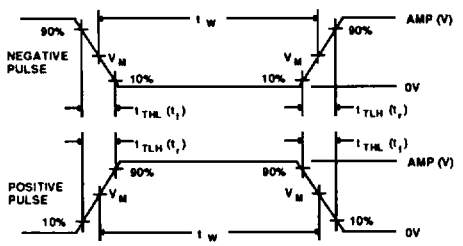
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns