



SN54LS195A SN74LS195A

DESCRIPTION — The SN54LS/74LS195A is a high speed 4-Bit Shift Register offering typical shift frequencies of 39 MHz. It is useful for a wide variety of register and counting applications. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL products.

- TYPICAL SHIFT RIGHT FREQUENCY OF 39 MHz
- ASYNCHRONOUS MASTER RESET
- J, \bar{K} INPUTS TO FIRST STAGE
- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

**UNIVERSAL 4-BIT
SHIFT REGISTER**
LOW POWER SCHOTTKY

PIN NAMES

\overline{PE}	Parallel Enable (Active LOW) Input
$P_0 - P_3$	Parallel Data Inputs
J	First Stage J (Active HIGH) Input
K	First Stage K (Active LOW) Input
CP	Clock (Active HIGH Going Edge) Input
\overline{MR}	Master Reset (Active LOW) Input
$Q_0 - Q_3$	Parallel Outputs (Note b)
\bar{Q}_3	Complementary Last Stage Output (Note b)

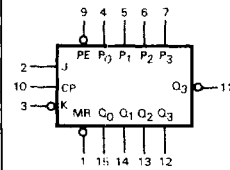
LOADING (Note a)

	HIGH	LOW
PE	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	0.5 U.L.	0.25 U.L.
J	0.5 U.L.	0.25 U.L.
K	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
\overline{MR}	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	10 U.L.	5(2.5) U.L.
\bar{Q}_3	10 U.L.	5(2.5) U.L.

NOTES:

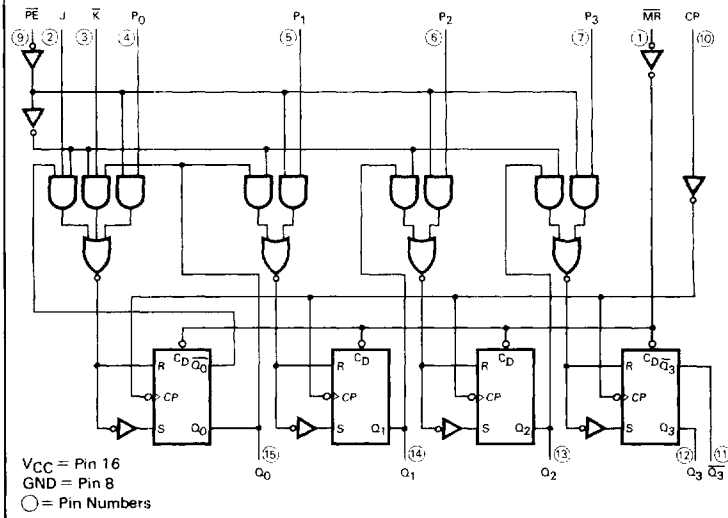
- 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL

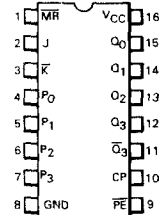


VCC = Pin 16
GND = Pin 8

LOGIC DIAGRAM



CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08
(Ceramic)
N Suffix — Case 648-05
(Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

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FUNCTIONAL DESCRIPTION — The Logic Diagram and Truth Table indicate the functional characteristics of the LS195A 4-Bit Shift Register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The LS195A has two primary modes of operation, shift right ($Q_0 \rightarrow Q_1$) and parallel load which are controlled by the state of the Parallel Enable (\overline{PE}) input. When the PE input is HIGH, serial data enters the first flip-flop Q_0 via the J and \overline{K} inputs and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW to HIGH clock transition. The \overline{JK} inputs provide the flexibility of the JK type input for special applications, and the simple D type input for general applications by tying the two pins together. When the \overline{PE} input is LOW, the LS195A appears as four common clocked D flip-flops. The data on the parallel inputs P_0, P_1, P_2, P_3 is transferred to the respective Q_0, Q_1, Q_2, Q_3 outputs following the LOW to HIGH clock transition. Shift left operations ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the P_{n-1} inputs and holding the \overline{PE} input LOW.

All serial and parallel data transfers are synchronous, occurring after each LOW to HIGH clock transition. Since the LS195A utilizes edge-triggering, there is no restriction on the activity of the J, \overline{K} , P_n and \overline{PE} inputs for logic operation — except for the set-up and release time requirements.

A LOW on the asynchronous Master Reset (\overline{MR}) input sets all Q outputs LOW, independent of any other input condition.

MODE SELECT — TRUTH TABLE

OPERATING MODES	INPUTS					OUTPUTS				
	\overline{MR}	\overline{PE}	J	\overline{K}	P_n	Q_0	Q_1	Q_2	Q_3	\overline{Q}_3
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	q_0	q_1	q_2	\overline{q}_2
Shift, Reset First Stage	H	h	l	l	X	L	q_0	q_1	q_2	\overline{q}_2
Shift, Toggle First Stage	H	h	h	l	X	\overline{q}_0	q_0	q_1	q_2	\overline{q}_2
Shift, Retain First Stage	H	h	l	h	X	q_0	q_0	q_1	q_2	\overline{q}_2
Parallel Load	H	l	X	X	P_n	p_0	p_1	p_2	p_3	\overline{p}_3

L = LOW voltage levels

H = HIGH voltage levels

X = Don't Care

l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition.

h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition.

P_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

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GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-0.4	mA
I_{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5	V	
V _{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	I _{OL} = 4.0 mA, V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74	0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
I _{IL}	Input LOW Current			0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IS}	Short Circuit Current	-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current			21	mA	V _{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
f _{MAX}	Maximum Clock Frequency	30	39		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH}	Propagation Delay Clock to Output		14	22	ns	
t _{PHL}	Propagation Delay MR to Output		17	26	ns	

AC SETUP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t _W	CP Clock Pulse Width	16			ns	V _{CC} = 5.0 V
t _W	MR Pulse Width	12			ns	
t _s	PE Setup Time	25			ns	
t _s	Data Setup Time	15			ns	
t _{rec}	Recovery Time	25			ns	
t _{rel}	PE Release Time			10	ns	
t _h	Data Hold Time	0			ns	

SETUP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

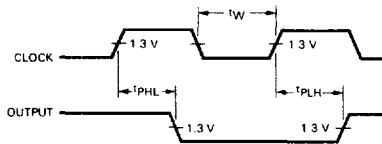
HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

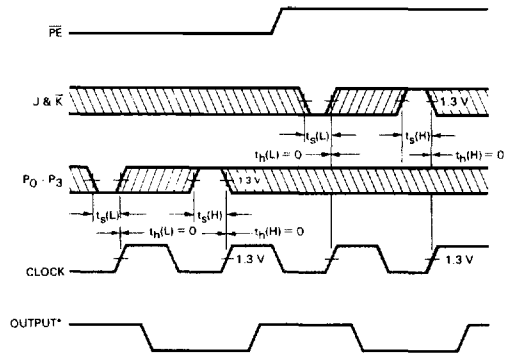
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



CONDITIONS: $J = \overline{PE} = \overline{MR} = H$
 $\overline{K} = L$

Fig. 1

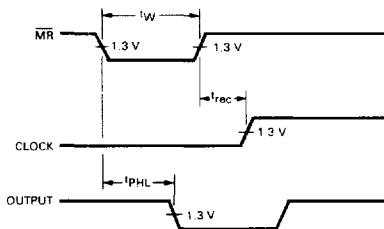
SETUP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (J & \overline{K}) AND PARALLEL DATA (P_0, P_1, P_2, P_3)



CONDITIONS: $\overline{MR} = H$
 * J and \overline{K} set-up time affects Q_0 only

Fig. 2

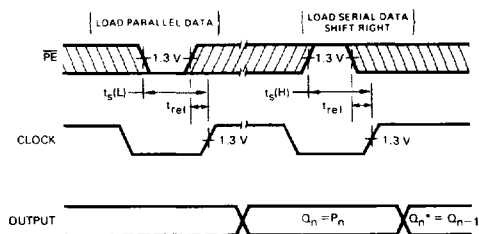
MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



CONDITIONS: $\overline{PE} = L$
 $P_0 = P_1 = P_2 = P_3 = H$

Fig. 3

SETUP (t_s) AND HOLD (t_h) TIME FOR \overline{PE} INPUT



CONDITIONS: $\overline{MR} = H$
 * Q_0 state will be determined by J and \overline{K} inputs

Fig. 4