

EXPANDABLE DUAL  
4-INPUT BUFFER

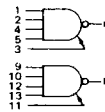
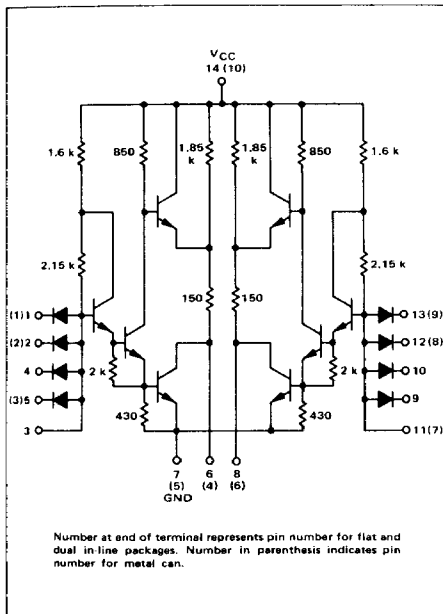
**MC932F • MC832F, P**

EXPANDABLE DUAL  
3-2 INPUT BUFFER

**MC932G • MC832G**

MDTL MC930/830 series

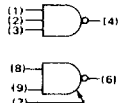
This buffer element, in the 14-pin flat and dual in-line packages, consists of two expandable 4-input inverting drivers. Since the metal can (G suffix) has only 10 pins, this circuit consists of one 3-input and one 2-input expandable inverting driver. These units are designed especially for driving large capacitive loads at high speeds. An output emitter follower in series with a 150-ohm resistor drives the output to the high voltage level. A low saturation resistance transistor is turned on, pulling the output down to the low voltage level, and providing rapid discharge of capacitive loads.



MC932F/MC832F, P

Positive Logic:  $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5} \cdot [3]$

Negative Logic:  $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5} \cdot [3]$



MC932G/MC832G

Positive Logic:  $4 = \overline{1 \cdot 2 \cdot 3}$

Negative Logic:  $4 = \overline{1 \cdot 2 \cdot 3}$

Input Loading Factor = 1

Output Loading Factor = 25

Total Power  
Dissipation.

MC932
MC832

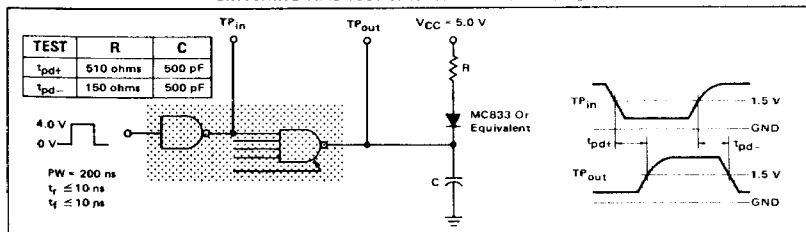
Inputs Low	12 mW
Inputs High	88 mW
50% Duty Cycle	50 mW

Propagation Delay Time = 35 ns typ

#### OPERATING RULES

- The outputs of the Dual Buffer may not be tied together.
- For increased current capability, the inputs and outputs of  $\frac{1}{2}$ MC932 and  $\frac{1}{2}$ MC944 can be paralleled (up to and including 4 common outputs). The combined output will equal 100 loads while each combined input will equal 4 loads.

#### SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



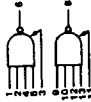
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MC932F/MC832F, P, (continued)  
 MC932G/MC832G (continued)

**ELECTRICAL CHARACTERISTICS**

Test procedures are shown for only one gate. The other gate is tested in the same manner.

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.



PACKAGE	PIN NUMBER													
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Flo/Dual In-Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Metal Can	1	2	-	-	-	-	-	-	-	-	-	-	-	-

Characteristic	Symbol	Pin Under Test	MC932 Test Limits														MC832 Test Limits														TEST CURRENT / VOLTAGE VALUES													
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C		-55°C		+25°C		+125°C		0°C		+25°C		-55°C		+25°C		+125°C		0°C		+25°C		+125°C									
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max								
Output Voltage	V <sub>OL</sub>	6	0.40	0.40	2.60	2.60	0.45	0.45	2.80	2.80	0.45	0.45	2.60	2.60	0.45	0.45	2.60	2.60	0.45	0.45	2.80	2.80	0.45	0.45	2.60	2.60	0.45	0.45	2.80	2.80	0.45	0.45	2.60	2.60	0.45	0.45								
	V <sub>OH</sub>	6	2.60	2.60	0.40	0.40	2.80	2.80	0.45	0.45	2.60	2.60	0.45	0.45	2.80	2.80	0.45	0.45	2.60	2.60	0.45	0.45	2.80	2.80	0.45	0.45	2.60	2.60	0.45	0.45	2.80	2.80	0.45	0.45	2.60	2.60								
Short-Circuit Current	I <sub>SC</sub>	6	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18	-18								
	I <sub>R</sub>	1	3.0	3.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0								
Output Leakage Current	I <sub>CEX</sub>	6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-								
	I <sub>F</sub>	1	-1.00	-1.00	-1.90	-1.90	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40	-1.40								
Power Drain Current (V <sub>OH</sub> Devices)	I <sub>PDH</sub>	14	-	-	26.6	26.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-								
	I <sub>max</sub>	14	-	-	6.0	6.0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-								
Switching Times	t <sub>pd+</sub>	1,6	-	-	25	25	80	80	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-								
	t <sub>pd-</sub>	1,6	-	-	15	15	40	40	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-								

Pins not listed are left open.

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## PRODUCT DOCUMENTATION

The three documents listed in the following table are required for a complete description of the DSP56301 and are necessary to design properly with the part. Documentation is available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

See the **Additional Support** section of the *DSP56300 Family Manual* for detailed information on the multiple support options available to you.

**Table 1** DSP56301 Documentation

Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD
DSP56301 User's Manual	Detailed functional description of the DSP56301 memory configuration, operation, and register programming	DSP56301UM/AD
DSP56301 Technical Data	DSP56301 features list and physical, electrical, timing, and package specifications	DSP56301/D

