

INCH-POUND
MIL-PRF-19500/108K
4 December 2006
SUPERSEDING
MIL-PRF-19500/108J
14 March 2006

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, THYRISTORS (CONTROLLED RECTIFIERS), SILICON,
TYPES 2N682, 2N683, 2N685 THROUGH 2N692, 2N692A, 2N5206, JAN AND JANTX

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for PNP silicon power, reverse-blocking triode thyristors. Two levels of product assurance are provided for each device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. See figure 1 (TO-208 stud, formerly TO-48).

1.3 Maximum ratings. $T_A = 25^\circ\text{C}$ unless otherwise stated.

	I_O (1)	I_{TSM} (2) $t = 7 \text{ ms}$	V_{GM}	T_J	T_{STG}	d_i/d_t (repetitive)
	<u>A</u>	<u>A</u>	<u>V (pk)</u>	<u>$^\circ\text{C}$</u>	<u>$^\circ\text{C}$</u>	<u>A/μs</u>
Min				-65	-65	5
Max	16	150	5	+125	+150	

- (1) This average forward current is for a maximum case temperature of $+65^\circ\text{C}$, and 180 electrical degrees of conduction.
- (2) Surge rating is non-recurrent and applies only with device in the conducting state. The peak rate of surge current must not exceed 100 amperes during the first 10 μs after switching from the off (blocking) state to the on (conducting) state. This time is measured from the point where the thyristor voltage has decayed to 90 percent of its initial blocking value.

Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dsc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://assist.daps.dla.mil/>.

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1.4 Primary electrical characteristics (common to all types).

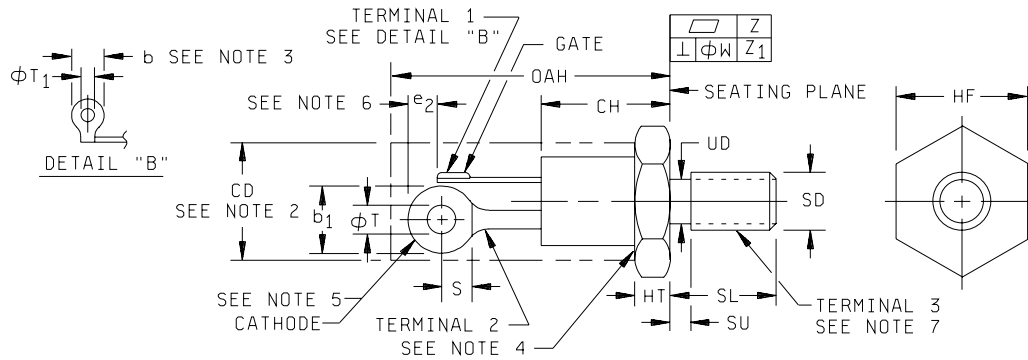
Limits	V_{TM}	I_H	V_{GT} (1)	I_{GT} (1)
	<u>V (pk)</u>	<u>mA dc</u>	<u>V dc</u>	<u>mA dc</u>
Min	2.0	50	0.25	80
Max			3.0	

(1) $T_C = -65^\circ\text{to } +125^\circ\text{C}$.1.4.1 Individual ratings.

Type	V_{RRM} (1)	V_{DRM}
	<u>V (pk)</u>	<u>V (pk)</u>
2N682	50	50
2N683	100	100
2N685	200	200
2N686	250	250
2N687	300	300
2N688	400	400
2N689	500	500
2N690	600	600
2N691	700	700
2N692	800	800
2N692A	800	800
2N5206	1,000	1,000

(1) Values apply for zero or negative gate voltage (V_{GM}).

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Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
b	.115	.139	2.92	3.53	3
b ₁	.210	.300	5.33	7.62	3
CD		.543		13.8	2
CH		.550		14.00	
e ₂	.125		3.17		6
HF	.544	.563	13.8	14.3	
HT	.075	.200	1.9	5.08	4
OAH		1.193		30.3	2
S	.120		3.05		3
SD	1/4 - 28 UNF 2A				
SL	.422	.453	10.7	11.5	
SU		.090		2.29	
ΦT	.125	.165	3.17	4.19	
ΦT ₁	.060	.075	1.52	1.9	
UD	.220	.249	5.59	6.32	

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Device contour, except on hex head and noted terminal dimensions, is optional within zone defined by CD and OAH, CD not to exceed actual HF.
3. Contour and angular orientation of terminals 1 and 2 with respect to hex portion and to each other are optional.
4. Chamfer or undercut on one or both ends of the hexagonal portion are optional.
5. Square or radius on end of terminal is optional.
6. Minimum difference in terminal lengths to establish datum line for numbering terminals.
7. Dimension SD is pitch diameter of coated threads.
8. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.

FIGURE 1. Physical dimensions (TO-208 stud, formerly TO-48).

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2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows:

V_{AA} - Anode power supply voltage (dc).

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figure 1 herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Lead material. Where a choice of lead material is desired, it shall be specified in the acquisition document (see 6.2).

3.4.3 Construction. These devices shall be constructed in a manner and using materials which enable the thyristors to meet the applicable requirements of MIL-PRF-19500 and this document.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

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3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I herein.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

* 4.3 Screening (JANTX level). Screening shall be in accordance with appendix E, table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement
	JANTX level
3a	Method 1051 of MIL-STD-750, condition F, 20 cycles.
10	Not required
11	I_{RRM1} , I_{DRM1} , V_{GT1} , V_{TM} , and I_{GT1}
12	Method 1040 of MIL-STD-750, condition A, $T_C = +125^\circ\text{C}$ minimum, $R_{GK} \geq 1\text{K } \Omega$; V_{DRM} , V_{RRM} = rated (see 1.4.1); .25 A or .125 A fuse may be used in accordance with method 1040 of MIL-STD-750.
13	Subgroup 2 of table I herein, $\Delta I_{RRM1} = 100$ percent of initial value or +0.4 mA (pk), whichever is greater. $\Delta I_{DRM1} = 100$ percent of initial value or +0.4 mA (pk), whichever is greater.
14a 14b	Required Method 1071 of MIL-STD-750, condition C or D for gross leaks.

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4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of table I, subgroups 1 and 2 inspection only (table E-VIb, group B, subgroup 1 of MIL-PRF-19500 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with appendix E, table E-V of MIL-PRF-19500, and table I herein.

4.4.2 Group B inspection (JAN and JANTX). Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIb (JAN and JANTX) of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with the applicable steps and footnotes of table II herein. Subgroups 3 and 6 of table E-VIb of MIL-PRF-19500, shall be performed on a sample from the subplot containing the highest voltage rated devices in the lot.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1037	ΔT_J between cycles $\geq +100^\circ\text{C}$; $t_{\text{on}} = t_{\text{off}} \geq 1$ minute for 2,000 cycles. No heat sink or forced air cooling on the device shall be permitted during the on state.
B3 (option 1)	1026	$T_C = 108^\circ\text{C} \pm 5^\circ\text{C}$, 50 minutes on, $I_O = 4$ A, T_C uncontrolled, 10 minutes off.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-VII of MIL-PRF-19500. Electrical measurements (end-points) requirements shall be in accordance with the applicable steps of table II herein.

4.4.3.1 Group C inspection, appendix E, table E-VII of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
C2	2036	Test condition A, weight = 10 pounds, duration = 15 seconds.
C6	1037	ΔT_J between cycles $\geq +100^\circ\text{C}$, $t_{\text{on}} = t_{\text{off}} \geq 1$ minute for 6,000 cycles. No heat sink or forced air cooling on the device shall be permitted during the on state.
C6 (option 1)	1026	$T_C = 108^\circ\text{C} \pm 5^\circ\text{C}$, 50 min on, $I_O = 4$ A, T_C uncontrolled, 10 minutes off.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

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TABLE I. Group A inspection.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Reverse blocking current	4211	AC method, bias condition D; f = 60 Hz, V_{RRM} = rated (see 1.4.1)	I_{RRM1}		2	mA (pk)
Forward blocking current	4206	AC method, bias condition D; f = 60 Hz; V_{DRM} = rated (see 1.4.1)	I_{DRM1}		2	mA (pk)
Gate trigger voltage and current	4221	$V_2 = V_D = 6$ V dc; $R_L = 50$ Ω ; $R_E = 20$ Ω maximum	V_{GT1} I_{GT1}		3 35	V dc mA dc
Forward on voltage	4226	$I_{TM} = 50$ A(pk) (pulse); pulse width = 8.5 ms; maximum; duty cycle = 2 percent maximum	V_{TM}		2	V (pk)
Holding current	4201	Bias condition D; $V_{AA} = 24$ V dc maximum; $I_{TM} = I_{F1} = 1$ A dc; $I_T = I_{F2} =$ 100 mA dc; trigger voltage source = 10 V; trigger PW = 100 μ s (minimum); $R_2 = 20$ Ω	I_H		50	mA dc
Reverse gate current	4219	$V_G = 5$ V dc	I_G		250	mA dc
<u>Subgroup 3</u>						
High temperature operation:		$T_C = +120^\circ\text{C}$ minimum				
Reverse blocking current	4211	AC method, bias condition D; f = 60 Hz; V_{RRM} = rated (see 1.4.1)	I_{RRM2}		5	mA (pk)
Forward blocking current	4206	AC method, bias condition D; f = 60 Hz; V_{DRM} = rated (see 1.4.1)	I_{DRM2}		5	mA (pk)

See footnote at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u> - Continued.						
Gate trigger voltage	4221	T _C = +120°C minimum; R _e = 20 Ω maximum	V _{GT2}	.25		V dc
2N682		V ₂ = V _{DM} = 50 V dc; R _L = 140 Ω				
2N683		V ₂ = V _{DM} = 100 V dc; R _L = 140 Ω				
2N685		V ₂ = V _{DM} = 200 V dc; R _L = 140 Ω				
2N686		V ₂ = V _{DM} = 250 V dc; R _L = 650 Ω				
2N687		V ₂ = V _{DM} = 300 V dc; R _L = 650 Ω				
2N688		V ₂ = V _{DM} = 400 V dc; R _L = 3 k Ω				
2N689		V ₂ = V _{DM} = 500 V dc; R _L = 3 k Ω				
2N690		V ₂ = V _{DM} = 600 V dc; R _L = 3 k Ω				
2N691		V ₂ = V _{DM} = 700 V dc; R _L = 3 k Ω				
2N692		V ₂ = V _{DM} = 800 V dc; R _L = 3 k Ω				
2N692A		V ₂ = V _{DM} = 800 V dc; R _L = 3 k Ω				
2N5206		V ₂ = V _{DM} = 1,000 V dc; R _L = 3 k Ω				
Low temperature operation:		T _C = -65°C maximum				
Reverse blocking current	4211	AC method, bias condition D; f = 60 Hz; V _{RRM} = rated (see 1.4.1)	I _{RRM3}		2	mA (pk)
Forward blocking current	4206	AC method, bias condition D; f = 60 Hz; V _{DRM} = rated (see 1.4.1)	I _{DRM3}		2	mA (pk)
Gate trigger voltage and current	4221	V ₂ = V _D = 6 V dc; R _L = 50 Ω; R _e = 20 Ω maximum	V _{GT3} I _{GT2}		3 80	V dc mA dc
<u>Subgroups 4 and 5</u>						
Not applicable						
<u>Subgroup 6</u>						
Surge current	4066	I _{TSM} = 150 A (pk) (half-sine wave); ten surges, one per minute; I _O = 16 A at rated V _{RRM} ; T _C = +65°C; f = 60 Hz; surge duration = 7 ms, minimum				
Electrical measurements		See table II, steps 1, 2, 3, 4, 5, and 6				

See footnote at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 7</u>						
Exponential rate of voltage rise	4231	Bias condition D; T _C = +120°C minimum, d _v /d _t = 25 v/μs; repetition rate = 60 pps; test duration = 15 s; C = 1.0 μF; R _L = 50 Ω	V _D			V dc
2N682		V _{AA} = 50 V dc		47		
2N683		V _{AA} = 100 V dc		95		
2N685		V _{AA} = 200 V dc		190		
2N686		V _{AA} = 250 V dc		240		
2N687		V _{AA} = 300 V dc		285		
2N688		V _{AA} = 400 V dc		380		
2N689		V _{AA} = 500 V dc		475		
2N690		V _{AA} = 600 V dc		570		
2N691		V _{AA} = 700 V dc		665		
2N692		V _{AA} = 800 V dc		760		
2N692A		V _{AA} = 800 V dc		760		
2N5206		V _{AA} = 1,000 V dc		950		
Circuit-commutated turn-off time	4224	T _C = +120°C minimum; I _{TM} = 10 A; t _{on} = 100 ±50 μs; d _i /d _t = 5 A/μs minimum; d _i /d _t = 8 A/μs maximum; reverse voltage at t ₁ = 15 V minimum; repetition rate = 60 pps maximum; d _i /d _t = 20 V/μs; gate bias conditions; gate source voltage = 0 V; gate source resistance = 100 Ω	t _{OFF}			
2N682		V _{DM} = V _{DRM} = 50 V (pk); V _{RRM} = 50 V maximum			30	μs
2N683		V _{DM} = V _{DRM} = 100 V (pk); V _{RRM} = 100 V maximum			30	μs
2N685		V _{DM} = V _{DRM} = 200 V (pk); V _{RRM} = 200 V maximum			30	μs
2N686		V _{DM} = V _{DRM} = 250 V (pk); V _{RRM} = 250 V maximum			30	μs
2N687		V _{DM} = V _{DRM} = 300 V (pk); V _{RRM} = 300 V maximum			30	μs
2N688		V _{DM} = V _{DRM} = 400 V (pk); V _{RRM} = 400 V maximum			30	μs
2N689		V _{DM} = V _{DRM} = 500 V (pk); V _{RRM} = 500 V maximum			40	μs
2N690		V _{DM} = V _{DRM} = 600 V (pk); V _{RRM} = 600 V maximum			40	μs
2N691		V _{DM} = V _{DRM} = 700 V (pk); V _{RRM} = 700 V maximum			60	μs
2N692		V _{DM} = V _{DRM} = 800 V (pk); V _{RRM} = 800 V maximum			60	μs
2N692A		V _{DM} = V _{DRM} = 800 V (pk); V _{RRM} = 800 V maximum			60	μs
2N5206		V _{DM} = V _{DRM} = 1,000 V (pk); V _{RRM} = 1,000 V maximum			60	μs
Gate controlled turn-on time	4223					
2N682, 2N683, 2N685 through 2N692 and 2N5206		V _{AA} = 50 V dc for 2N682, 100 V dc for 2N683 and 2N685 through 2N692 and 2N5206; I _{TM} = 10 A dc; V _{GG} = 10 V dc; R _e = 25Ω; t _{p1} = 15 ±5 μs; 4 A/μs ≤ d _i /d _t ≤ 200 A/μs.	t _{on}		5	μs
2N692A					.5	μs

1/ For sampling plan, see MIL-PRF-19500.

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TABLE II. Groups A, B, and C electrical end-point inspection measurements. 1/ 2/

Step	Inspection	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
1.	Reverse blocking cutoff current	4211	AC method, bias condition D; f = 60 Hz; V_{RRM} = rated	I_{RRM1}		2	mA (pk)
2.	Forward blocking current	4206	AC method, bias condition D; f = 60 Hz; V_{DMR} = rated	I_{DRM1}		2	mA (pk)
3.	Reverse blocking cutoff current	4211	AC method, bias condition D; T_C = +120°C minimum; f = 60 Hz; V_{RRM} = rated	I_{RRM2}		5	mA (pk)
4.	Forward blocking current	4206	AC method, bias condition D; T_C = +120°C minimum; f = 60 Hz; V_{DMR} = rated	I_{DRM2}		5	mA (pk)
5.	Gate-trigger voltage and current	4221	$V_2 = V_D = 6$ V dc; $R_L = 50 \Omega$; $R_E = 20 \Omega$ maximum	V_{GT1} I_{GT1}		3 35	V dc mA dc
6.	Forward on voltage transfer ratio	4226	$I_{TM} = 50$ A (pk) (pulse); pulse width = 8.5 ms maximum; duty cycle = 2 percent maximum	V_{TM}		2.0	V (pk)

1/ The electrical measurements for table E-VIb (JAN and JANTX) of MIL-PRF-19500 are as follows: Subgroups 2, 3, and 6, see table II herein, steps 1, 2, 3, 4, 5, and 6.

2/ The electrical measurements for table E-VII of MIL-PRF-19500 are as follows: Subgroups 2, 3, and 6, see table II herein, steps 1, 2, 3, 4, 5, and 6.

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5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish and material (see 3.4.1 and 3.4.2).
- d. Product assurance level and type designator.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML-19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

6.4 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR
Navy - EC
Air Force - 11
DLA - CC

Preparing activity:

DLA - CC

(Project 5961-2006-093)

Review activities:

Army - AR, AV, MI, SM
Navy - AS, MC
Air Force - 19, 99

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