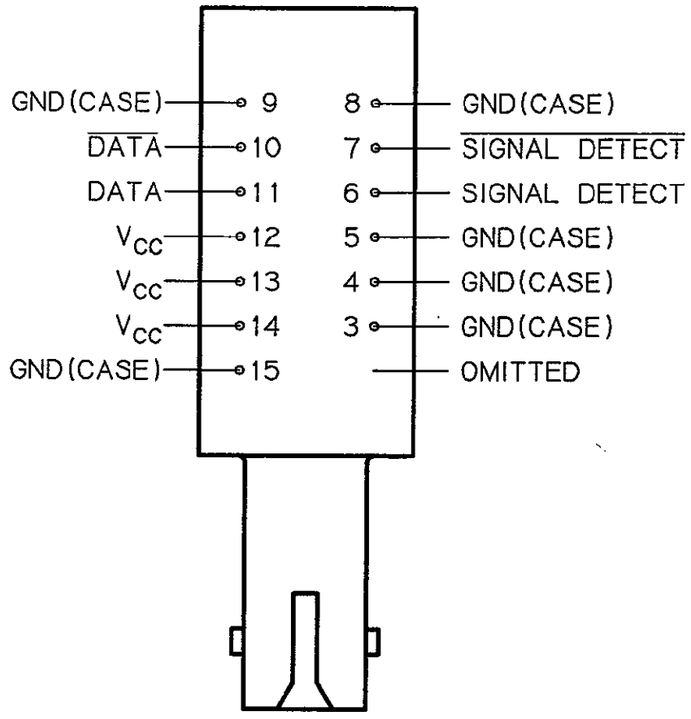
LOC	DIST
DR	01

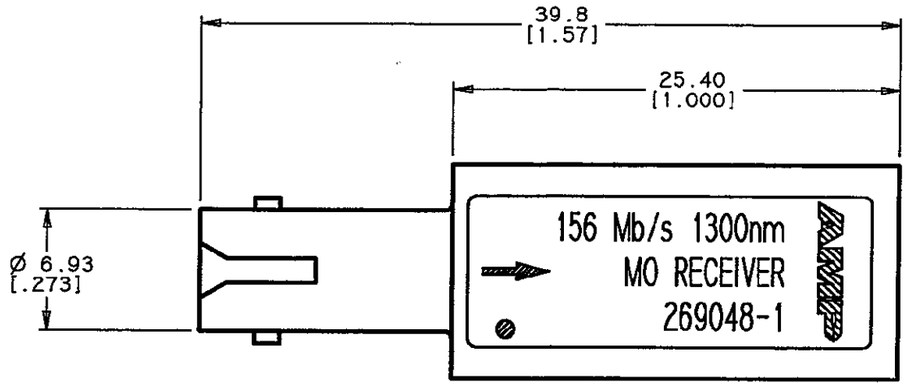
REVISIONS

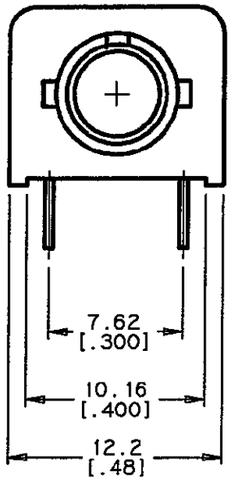
P	LTR	DESCRIPTION	DATE	DWN	APVD
	C	EC 0D30-0052-99	22FEB99	PEM	

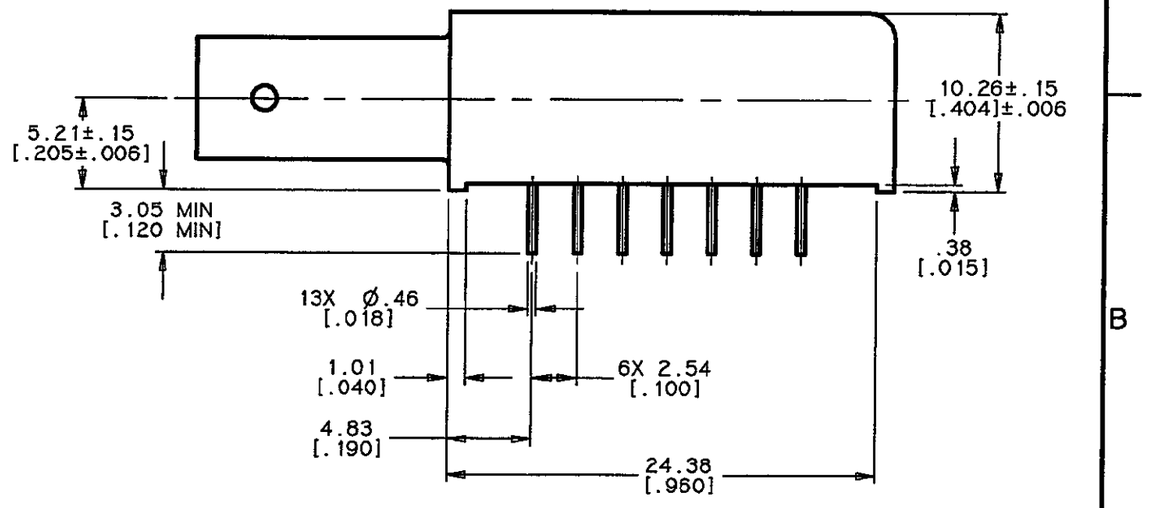


PINOUT WHEN VIEW FROM TOP

RAISED ECL V_{EE} = GND
V_{CC} = +5V ±5%







NOTES:

1. DIMENSIONS IN [ ] ARE IN INCHES.
2. PIN PLATING: 100 MICROINCHES Sn93Pb7 OVER 50 MICROINCHES Ni SOLDER DIPPED IN Sn90Pb10.
3. 0ns EYE OPENING, V_{CC} =5V, 25°C, 2^{23} -1 PRBS.
4. VOLTAGE LEVELS LISTED ARE COMPATIBLE WITH 100K SERIES ECL LOGIC LEVELS. THE PARTS ARE 100% COMPATIBLE WITH 10K AND 10KH SERIES LOGIC WHEN DRIVEN WITH DIFFERENTIAL SIGNALS.
5. UNIT PROVIDED WITH PROCESS CAP TO PROTECT OPTICAL PORTS DURING SOLDERING AND CLEANING PROCESSES.

THIS DRAWING IS A CONTROLLED DOCUMENT FOR AMP INCORPORATED. IT IS SUBJECT TO CHANGE AND THE CONTROLLING ENGINEERING ORGANIZATION SHOULD BE CONTACTED FOR THE LATEST REVISION.

DIMENSIONS: mm [Inches]

TOLERANCES UNLESS OTHERWISE SPECIFIED:
1 PLC. DEC. ±0.25 [.010]
2 PLC. DEC. ±0.13 [.005]
ANGLES ±0.5 DEG.

MATERIAL:

FINISH:

DWN. P. MALARCHER
CHK. L. JACOB
APVD Paul Malarcher 22Feb99
PRODUCT SPEC. 108-55003
APPLICATION SPEC. -
WEIGHT. -
CUSTOMER DRAWING

AMP Incorporated
Harrisburg, PA 17105-3608

NAME
RECEIVER MODULE
MOLDED OPTICS, 16 PIN
2.5mm BAYONET, 156 Mb/s PD\3111CC

SIZE	CAGE CODE	DRAWING NO.
A3	-	C-269048-1

SCALE: 3:1 SHEET 1 OF 2 REV. C

LOC	DIST
DR	01

REVISIONS

P	LTR	DESCRIPTION	DATE	DWN	APVD
	C	EC 0D30-0052-99		PEM	

PERFORMANCE SPECIFICATIONS (T_A = 0-70°C, V_{CC} - V_{EE} = 4.75-5.25V DC)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DATA RATE (NRZ)	B	-	10	-	156	Mb/s
OPTICAL INPUT (AVG) SENSITIVITY (3)	P_{IN}	0.275NA 62.5/125µm FIBER B=156Mb/s, BER=$1.0X10^{-10}$	-33.3	-	-14.0	dBm
OPTICAL WAVELENGTH	λ_{IN}	-	1270	-	1380	nm
DUTY CYCLE	-	-	25	50	75	%
OUTPUT RISETIME	t_{TLH}	20-80%, 50Ω TO V_{CC}-2V	.5	-	2.5	ns
OUTPUT FALLTIME	t_{THL}	80-20%, 50Ω TO V_{CC}-2V	.5	-	2.5	ns
PULSE WIDTH DISTORTION	-	50Ω TO V_{CC}-2V	-	-	0.4	ns
DATA DEPENDENT JITTER	t_{DDJ}		-	-	0.8	ns
OUTPUT VOLTAGE LEVELS (OUTPUT) (4)	V_{OH}	$P_{IN} \geq P_A$	V_{CC}-1.025	-	V_{CC}-.88	V
	V_{OL}	$P_{IN} \geq P_A$	V_{CC}-1.81	-	V_{CC}-1.62	V
SIGNAL DETECT (OUTPUT)	V_A	$P_{IN} \geq P_A$, 50Ω TO V_{CC}-2V	V_{CC}-1.025	-	V_{CC}-.88	V
	V_D	$P_{IN} < P_D$, 50Ω TO V_{CC}-2V	V_{CC}-1.81	-	V_{CC}-1.62	V
P_{IN} POWER LEVELS (AVG)						
DEASSERT	P_D		-39	-	-32.5	dBm
ASSERT	P_A		-38	-	-31.0	dBm
HYSTERESIS			1.5	2.0	-	dB
SIGNAL DETECT DELAY TIME						
DEASSERT		-	-	-	50	µs
ASSERT		-	-	-	50	µs
POWER SUPPLY VOLTAGE	V_{CC} - V_{EE}	-	4.75	5.0	5.25	V
SUPPLY CURRENT	I_{CC} OR I_{EE}	-	-	-	150	mA
OPERATING TEMPERATURE	T_A	-	0	-	70	°C
ABSOLUTE MAXIMUM RATINGS						
STORAGE TEMPERATURE	-	-	-40	-	100	°C
LEAD SOLDERING LIMITS	-	-	-	-	240/10	°C/s
POWER SUPPLY VOLTAGE	V_{CC} - V_{EE}	-	-.2	-	7.00	V

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RECEIVER MODULE
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2.5mm BAYONET, 156 Mb/s

SIZE A3 | CAGE CODE - | DRAWING NO. C-269048-1
SCALE: 3:1 | SHEET 2 OF 2 | REV. C

FD\3112DCC